CLAIMS

WHAT IS CLAIMED:

1. An apparatus, comprising:

a first doped region;

a first doped well disposed within the first doped region;

a first doped plug disposed within the first doped well;

a second doped plug disposed within the first doped region; and

an isolation structure disposed between the first and second doped plugs.

2. The apparatus of claim 1, further comprising a second doped well disposed within the first doped region, wherein the second doped plug is disposed within the second doped well.

3. The apparatus of claim 1, wherein a first breakover voltage exists between the first doped well and the first doped region, a second breakover voltage exists between the first doped plug and the first doped region, the location of the first doped plug inside the first doped well determines the second breakover voltage, and the second breakover voltage is less than the first breakover voltage.

4. The apparatus of claim 3, wherein the first doped plug has a first boundary the first doped well has a second boundary, and the second breakover voltage is dependent on the proximity of the first boundary to the second boundary.

5. The apparatus of claim 2, wherein the second doped well has a first boundary, the second doped plug has a second boundary, and the second boundary is proximate the first boundary.

6. The apparatus of claim 1, wherein the isolation structure is at least one of a LOCOS oxide and a surface trench filled with an oxide.

7. The apparatus of claim 1, wherein the isolation structure is a gate terminal comprising a dielectric layer disposed adjacent to at least a portion of the first doped region and a conductor layer disposed above at least a portion of the dielectric layer.

8. The apparatus of claim 1, further comprising a conductor layer disposed above at least a portion of the first and second doped plugs.

9. The apparatus of claim 1, wherein the first doped region comprises a p-type material.

10. The apparatus of claim 1, wherein the first and second doped plugs comprise an n-type material.

11. The apparatus of claim 2, wherein the first and second doped wells comprise an n-type material, and the doping concentrations of the first and second doped wells are less than the doping concentrations of the first and second doped plugs.

12. The apparatus of claim 3, wherein the second breakover voltage is within a range of about 10-50V.

13. An apparatus comprising:

a p-type semiconductor substrate;

a first n-well disposed within the semiconductor substrate;

a first n-plug disposed within the first n-well;

a second n-plug disposed within the p-type semiconductor substrate; and

an isolation structure disposed between the first and second n-plugs.

14. The apparatus of claim 13, further comprising a second n-well disposed within the p-type semiconductor substrate, wherein the second n-plug is disposed within the second n-well.

15. The apparatus of claim 14, wherein the second n-well has a first boundary, the second n-plug has a second boundary, and the second boundary is proximate the first boundary.

16. The apparatus of claim 13, wherein a first breakover voltage exists between the first n-well and the p-type semiconductor substrate, a second breakover voltage exists between the first n-plug and the p-type semiconductor substrate, the location of the first n-plug inside the first n-well determines the second breakover voltage, and the second breakover voltage is less than the first breakover voltage.

17. The apparatus of claim 16, wherein the first n-plug has a first boundary, the first n-well has a second boundary, and the second breakover voltage is dependent on the proximity of the first boundary to the second boundary.

18. The apparatus of claim 13, wherein the isolation structure is at least one of a LOCOS oxide and a surface trench filled with an oxide.

19. The apparatus of claim 13, wherein the isolation structure is a gate terminal comprising a dielectric layer disposed adjacent to at least a portion of the first doped region and a conductor layer disposed above at least a portion of the dielectric layer.

20. The apparatus of claim 16, wherein the second breakover voltage is within a range of about 10-50V.

21. A integrated circuit, comprising:

an external bond pad;

a voltage source;

an ESD protection device coupled between the external bond pad and the voltage source, wherein the ESD protection device comprises:

a first doped region;

a first doped well disposed within the first doped region;

a first doped plug disposed within the first doped well and coupled to the external bond pad;

a second doped plug disposed within the first doped region and coupled to the voltage source; and

an isolation structure disposed between the first and second doped plugs; and

at least one integrated component coupled to the ESD protection device.

22. The integrated circuit of claim 21, wherein the ESD protection device further comprises a second doped well disposed within the first doped region, wherein the second doped plug is disposed within the second doped well.

23. The integrated circuit of claim 21, wherein the ESD protection device comprises a first breakover voltage between the first doped well and the first doped region, a second break-over voltage between the first doped plug and the first doped region, the location of the first doped plug inside the first doped well determines the second breakover voltage, and the second breakover voltage is less than the first breakover voltage.

24. The integrated circuit of claim 23, wherein the first doped plug of the ESD protection device has a first boundary, the first doped well has a second boundary, and the second breakover voltage is dependent on the proximity of the first boundary to the second boundary.

25. The integrated circuit of claim 22, wherein the second doped well of the ESD protection device has a first boundary, the second doped plug has a second boundary, and the second boundary is proximate the first boundary.

26. The integrated circuit of claim 21, wherein the isolation structure of the ESD protection device is at least one of a LOCOS oxide and a surface trench filled with an oxide.

27. The integrated circuit of claim 21, wherein the first doped region of the ESD protection device comprises a p-type material.

28. The integrated circuit of claim 21, wherein the first and second doped plugs of the ESD protection device comprise an n-type material.

29. The integrated circuit of claim 21, wherein the first and second doped wells of the ESD protection device comprise an n-type material, and the doping concentrations of the first and second doped wells are less than the doping concentrations of the first and second doped plugs.

30. The integrated circuit of claim 23, wherein the second breakover voltage of the ESD protection device is within a range of about 10-50V.

31. The integrated circuit of claim 21, wherein the voltage source is coupled to ground.

32. The integrated circuit of claim 21, wherein the voltage source is coupled to a power supply.

33. The integrated circuit of claim 21, further comprising a buffer coupled between the ESD protection device and the integrated components.

34. The integrated circuit of claim 21, wherein the integrated component is an anti-fuse network.

35. A method, comprising:

providing a first doped region;

forming a first doped well within the first doped region;

forming a first doped plug into the first doped region;

forming a second doped plug into the first doped region; and

forming an isolation structure between the first and second doped plugs.

36. The method of claim 35, further comprising forming a second doped well within the first doped region, wherein forming the second doped plug includes forming the second doped plug in the second doped well.

37. The method of claim 35, wherein forming the first doped plug includes forming the first doped plug a first distance from a first boundary of the first doped well, and a breakover voltage between the first doped plug and the first doped region depends on the first distance.

38. The method of claim 35, wherein forming the isolation structure includes forming at least one of a LOCOS oxide and a surface trench filled with an oxide.

39. The method of claim 35, wherein forming the isolation structure includes forming a gate terminal.

40. The method of claim 39, wherein forming the gate terminal includes:

forming a dielectric layer adjacent to at least a portion of the first doped region; and

forming a conductor layer above at least a portion of the dielectric layer.

41. The method of claim 35, further comprising forming a conductor layer above at least a portion of the first and second doped plugs.

42. The method of claim 35, wherein providing the first doped region comprises providing a p-type first doped region.

43. The method of claim 35, wherein forming the first and second doped plugs comprises forming n-type first and second doped plugs.